Overview

FW1935 is a dedicated circuit for single-wire 3-channel LED constant current drive. Its input can be achieved through the mutual switching of the two-channel digital interfaces (DIN, FDIN) which are cascaded with DO port. The external controller only needs a single wire to control the chip which integrates with MCU single-wire two-channel digital interface, data latch, LED constant current drive, PWM luminance control and other circuits. VDD pin integrates with 5V voltage-regulator tube, with few peripheral devices. The product applies to guardrail tube, point light source and other LED decoration products. It boasts excellent performance and reliable quality.

Features

- Low power consumption CMOS workmanship
- OUT output port withstand voltage 24V
- VDD has built-in 5V voltage-regulator tube, supporting 6-24V voltage after connected in series with resistors
- 15mA fixed constant current output
- PWM luminance control circuit, 256-level luminance control
- Accurate current output value
  Maximum error (between channels): ±3%
  Maximum error (between chips): ±5%
- Single-wire serial cascaded interface
- Single-wire two-channel serial concatenated interface: The chip data interface can configure DIN or FDIN pin input through the command. In normal mode, the input interfaces switch with each other. In DIN operating mode, DIN pin inputs data. In FDIN operating mode, FDIN pin inputs data. D0 pins forward cascaded data. The signal does not affect the normal operation of other chips because of the abnormity of a certain chip.
- Oscillation mode: built-in RC oscillation, clock synchronization according to the signals on the data line, automatically regenerate the subsequent data after receiving the data of the current unit and send it to the next level through the data output end, the signals do not distort or attenuate with the farther distance of cascade connection
- Built-in power-on reset circuit, all registers are zero-initialized after power-on reset
- Data transmission rate 800KHz
- Packaging mode: SOP8

Block diagram for internal structure

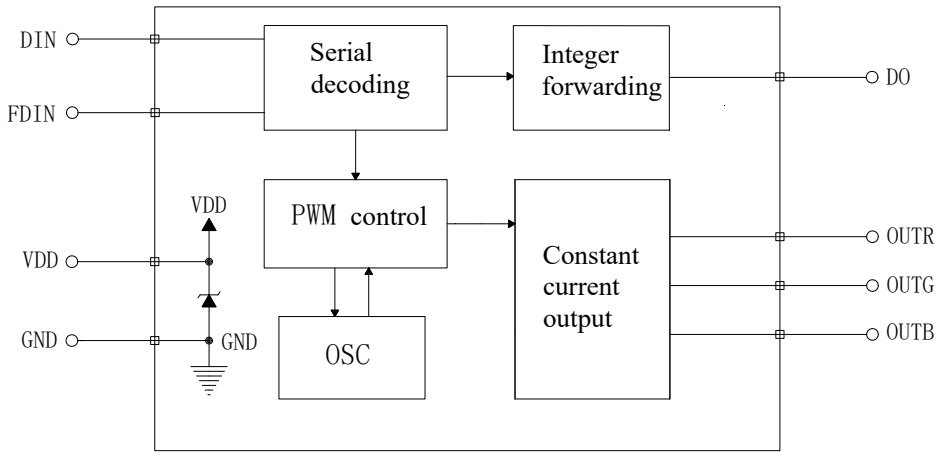


Figure 1

Configuration of SOP8 pins

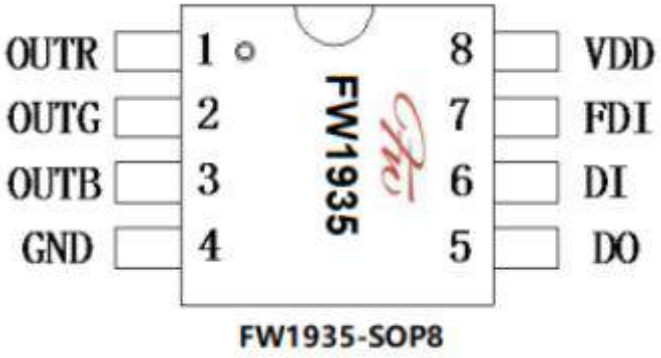


Figure 2

Pin function

Pin name	Pin number	I/O	Function description
DI	6	I	Data input
FDI	7	I	Backup data input
DO	5	O	Data output
OUTR	1	O	N tube open-drain, constant-current output
OUTG	2	O	N tube open-drain, constant-current output
OUTB	3	O	N tube open-drain, constant-current output
VDD	8	--	Positive pole of power supply
GND	4	--	Power ground

Input/output equivalent circuit

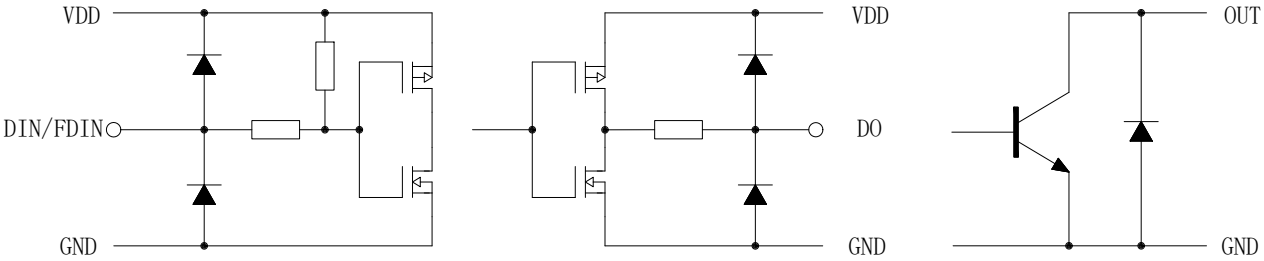


Figure 3

Integrated circuit is an electrostatic sensitive device which tends to generate a lot of static electricity when used in a dry season or dry environment. Electrostatic discharge may damage integrated circuit. Titan Micro Electronics suggests taking all appropriate preventive measures for integrated circuit. Improper operation and welding might cause ESD damage or performance reduction and chip operation failure.

Limit parameters

Parameter name	Parameter symbol	Limit value	Unit
Logic supply voltage	VDD	-0.4～+7.0	V
Voltage of DIN and FDIN ports	Vin	-0.4～VDD+0.7	V
OUT port voltage	Vout	-0.4～+32.0	V
Operating temperate range	Topr	-40～+85	℃
Storage temperature range	Tstg	-50～+150	℃
ESD	Human body model (HBM)	3000	V
	Machine model (MM)	300	V

(1) When the chip works for a long time under the above limit parameters, it may cause device reliability reduction or permanent damage. We do not suggest the chip works by exceeding these limit parameters under any other conditions.
(2) All voltage values are comparatively tested in a systematic way.

Recommended operating conditions

Tested under -45℃-+85℃, unless otherwise specified			FW1935			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
Supply voltage	VDD		4.5	5.0	6.5	V
Voltage of DIN and FDIN ports	Vin	VDD=5V, DIN and FDIN are connected in series with a 1KΩ resistor			VDD+0.4	V
Voltage of DO ports	Vdo	VDD=5V, DO are connected in series with a 1KΩ resistor			VDD+0.4	V
SET port voltage	Vset	VDD=5V			VDD+0.4	V
OUT port voltage	Vout	OUT＝OFF			24.0	V

Electrical characteristics

Tested under VDD=3.0-5.5V and operating temperature = -40℃-+85℃, unless otherwise specified			FW1935			Unit
Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	
High level output voltage	Voh	Ioh=3mA	VDD-0.5			V
Low level output voltage	Vol	Iol=10mA			0.4	V
High level input voltage	Vih	VDD=5.0V	3.5		VDD	V
Low level input voltage	Vil	VDD=5.0V	0		1.5	V
High level output current	Ioh	VDD=5.0V, Vdo=4.9V		1		mA
Low level output current	Iol	VDD=5.0V, Vdo=0.4V		10		mA
Input current	Iin	DIN and FDIN connect with VDD		1		μA
Quiescent current	IDD	VDD=4.0V, GND=0V, other ports are suspended	0.5	1.2	1.5	mA
OUT output constant current	Iout	OUTR, OUTG, OUTB=ON, Vout=3.0V	14	15	16	mA
OUT output leakage current	Iolkg	OUTR, OUTG, OUTB=OFF, Vout=24.0V			0.5	μA
Constant-current error between channels	ΔIolc0	OUTR, OUTG, OUTB=ON, Vout=3.0V			±3	%
Constant-current error between chips	ΔIolc1	OUTR, OUTG, OUTB=ON, Vout=3.0V			±5	%
Consumed power	Pd	Ta=25℃			250	mW

Switch characteristics

Tested under VDD=3.0-5.5V and operating temperature = -40℃-+85℃, typical value VDD=5.0V, TA=+25℃, unless otherwise specified			FW1935			Unit
Parameter name	**Parameter symbol**	**Testing condition**	**Min. value**	**Typical value**	**Max. value**	
Data rate	Fin			800		KHz
OUT PWM output frequency	Fout	OUTR, OUTG, OUTB		1000		Hz
Propagation delay time	Tplz	DIN → DO FDIN → DO		155		ns
Input capacitance	Ci				15	pF

Time sequence characteristics

Parameter name	Parameter symbol	Testing condition	Min. value	Typical value	Max. value	Unit
Input 0 ode, high level time	T0H	VDD=5.0V GND=0V	310	360	410	ns
Input 1 ode, high level time	T1H		650	720	1000	ns
Output 0 ode, high level time	T0H’			350		ns
Output 1 ode, high level time	T1H’			700		ns
0 code or 1 code cycle	T0/T1			1.25		μs
Reset code, low level time	Treset		200			μs

(1) When 0 code or 1 code cycle is within the range of 1.25μs (frequency 800KHz) to 2.5μs (frequency 400KHz), the chip can normally work, but the low level time of 0 code and 1 code must accord with the corresponding values in the above table;
(2) When reset is not required, the low level time between bytes should not exceed 50μs, or else the chip may be rest to receive data again, which cannot achieve correct data transmission.

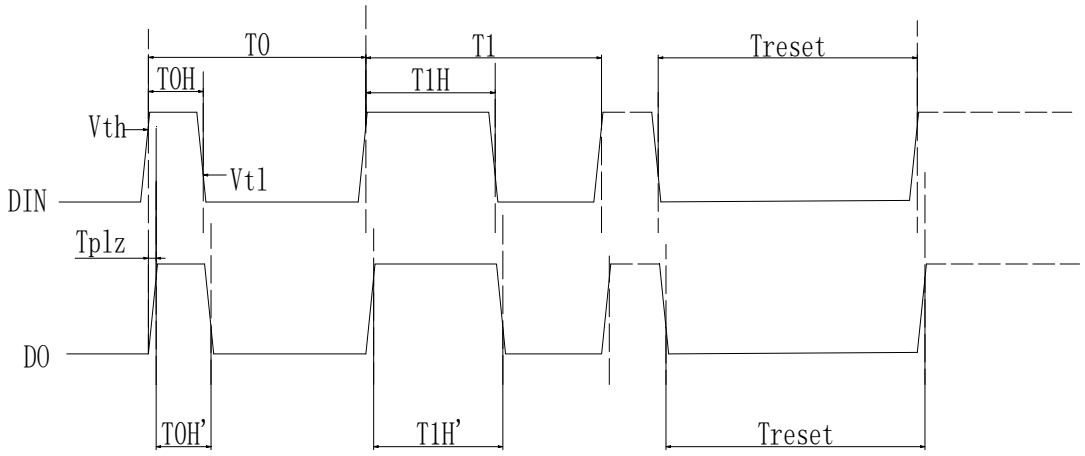


Figure 4

Function description

1. Display data

After power-on reset and reception of a mode setting command, the chip begins to receive display data. When the 24-bit data are received, DO ports will start to forward the data continuously sent from DIN or FDIN port, which provides display data for the next cascaded chip. Prior to forwarding data, DO ports are always at low level. If DIN or FDIN port is input with Reset signals, chip OUT port will output the PWM waveform of corresponding duty ratio according to the received 24-bit data, and the chip will wait to receive new data again. Upon receiving the initial 24-bit data, DO port will forward the data. Before the chip receives no Reset signal, the original output of OUTR, OUTG and OUTB remains unchanged.

The chip adopts auto integer forwarding technology, so that the signals will not distort and attenuate. For all the cascaded chips, the cycles of data transmission are consistent.

2. Structure of a complete frame of data

D1	D2	D3	D4	···	Dn	Reset	D1	D2	D3	D4	···	Dn	Reset

The data formats of D1, D2, D3, D4,…Dn are the same, wherein D1 means the display data packet of the first cascaded chip and Dn means the data display packet of the n^{th} cascaded chip. Each display data packet contains 24 data bits. Reset means reset signal, valid at low level.

3. Data format of Dn

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Each data packet contains 8×3 data bits, with higher bits sent first.

R[7:0]: used to set the PWM duty ratio output by OUTR. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.

G[7:0]: used to set the PWM duty ratio output by OUTG. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.

B[7:0]: used to set the PWM duty ratio output by OUTB. Full 0 code is off, full 1 code is of maximum duty ratio, 256-level adjustable.

4. Data reception and forwarding

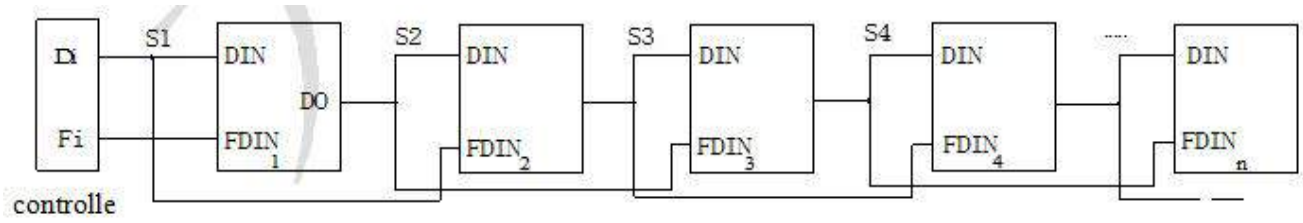


Figure 5

Annotation: If the controller is only one port signal, the first point of FDIN impending, DIN is connected to the controller, the other click the above link

Wherein, S1 is the data sent by Di port of the controller, S2, S3 and S4 are the data forwarded by cascaded FW1935.

Data structure of Di and Fi2 ports of the controller: D1D2D3D4……Dn;

Data structure of Fi port of the controller: DxD1D2D3……Dn;

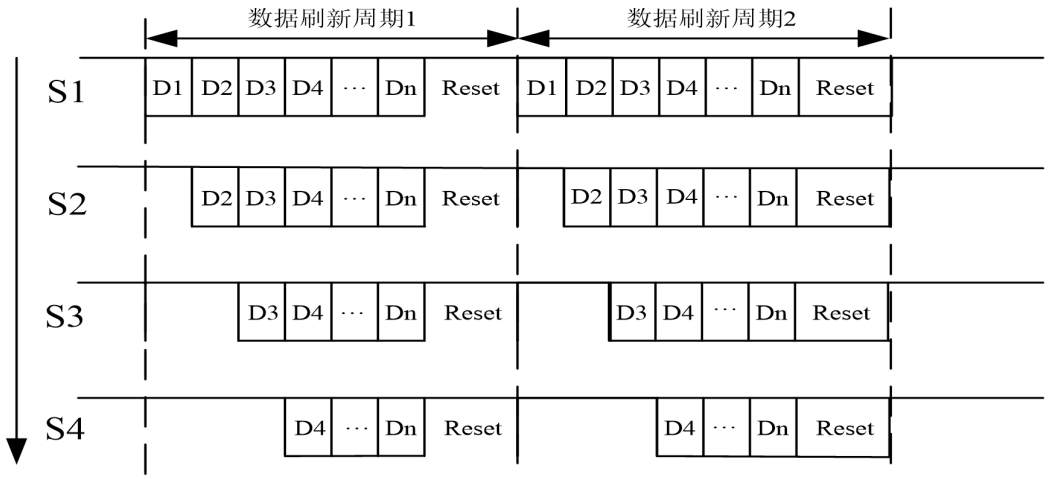


Figure 6

The data transmission and forwarding process when chips are cascaded is as follows: controller sends packetD1, Chip 1 receives the first set of 24bit,At this time, chip 1 has no forwarding;Then the controller sends the packet D2,Chip 1 receives the second set of 24 bits,Since the chip 1 already has the first set of 24 bits,Therefore, the chip 1 forwards the second group 24 bits to the chip 2 through the DO.The chip 2 receives the data packet D2 forwarded by the chip 1,At this time, chip 2 has no forwarding;The controller then sends the packet D3,Chip 1 forwards the received third set of 24 bits to chip 2,Since the chip 2 already has a second set of 24 bits,Therefore, the chip 2 forwards the third group 24bit to the chip 3, and the chip 3 receives the third group 24bit; and so forth, until the controller sends Reset signal, all the chips will reset and control the received 24-bit data to output them from OUT port after decoding, which completes a data refresh cycle and makes the chips return to the reception-ready state. Reset is valid at low level. To make the chip reset, the low level time should be maintained at more than 200μs.

Application information

1. Typical application circuit

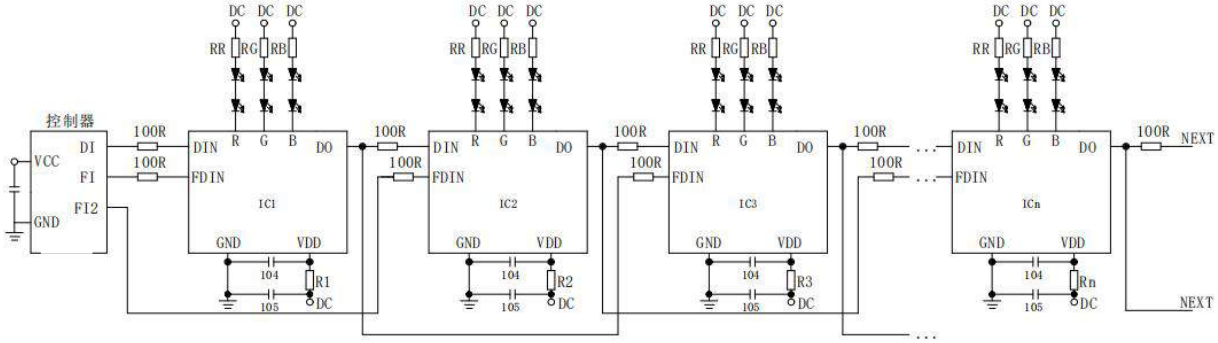


Figure 7

Annotation: If the controller is only one port signal, the first point of FDIN impending, DIN is connected to the controller, the other click the above link

To prevent chip signal input/output pin damage caused by the transient peak voltage generated by hot plugging when the product is tested, 100Ω protective resistors should be connected in parallel at signal input and output pins. Besides, the 104 decoupling capacitance of each chip in the figure is indispensable, and the wiring to the VDD and GND pins of the chips should be as short as possible, in order to achieve optimal decoupling effect and stable chip operation.

2. Power configuration

FW1935 can be configured with DC6-24V power supply, but different power resistors should be configured according to different input voltages. Calculation method of resistance: when the current of VDD port is 10mA, VDD series resistance R= (DC-5.5V) ÷10mA (DC is supply voltage).

Typical values of configured resistors are as shown in the following table:

Supply voltage (DC)	Suggested power interface and VDD series resistance value
5V	No need of connection of resistors, internal voltage-regulator tube malfunctions
12V	1KΩ
24V	2.4KΩ

3. Functions of different operating modes

In the process of normal use, the chips should be set as normal operating mode. To switch data input throughDIN and FDIN and data output through DO can effectively prevent abnormal transmission of data caused by the damage of the data input or output port of a chip or the damage of the entire chip.

In the process of aging and installation, the chips can be set as DIN operating mode and FDIN operating mode to test the chips and their wire connectivity, in a way to discover chip damage, bad wire connection or other hidden dangers in a timely manner.

4. How to calculate the data refresh rate

The data refresh time is calculated according to how many pixel points are cascaded in one system. A set of RGB is usually a pixel (or a segment), a FW1935 chip can control a set of RGB.

Calculated according to the normal mode:

1-bit data cycle is 1.25μs (frequency 800KHz), and 1-pixel data contains R (8bits), G (8bits) and B (8bits), totally 24 bits. The transmission time is 1.25μs×24=30μs. If one system contains 1,000 pixel points, the time for refreshing full display once is 30μs×1000=30ms (omitting C1, C2 and Reset signal time), i.e., the refresh rate of one second is: 1÷30ms≈33Hz.

The following table shows the highest data refresh rates corresponding to cascaded pixel points:

	Normal mode	
Pixel points	Fastest time for refreshing data once (ms)	Highest data refresh rates (Hz)
1～400	12	83

1～800	24	41
1～1000	30	33

5. How to make FW1935 work under optimal constant current state

The SET pin connected to GND of FW1935 applies to constant current drive. According to the constant current curve, when OUT port voltage reaches 0.8V, FW1935 will enter the constant current state. However, it does not mean it is better when the voltage is higher, because when the voltage is higher, the power consumption of the chip will be larger and the heating will be more serious, which lowers the reliability of the whole system. It is suggested that the voltage is 1.5-3V when OUT port is opened. Series resistance can be adopted to lower the excessive voltage of OUT port. The following is the calculation method for selecting resistance values:

System drive voltage: DC

Single LED breakover voltage drop: Vled

Series LED number: n

Constant current value: Iout

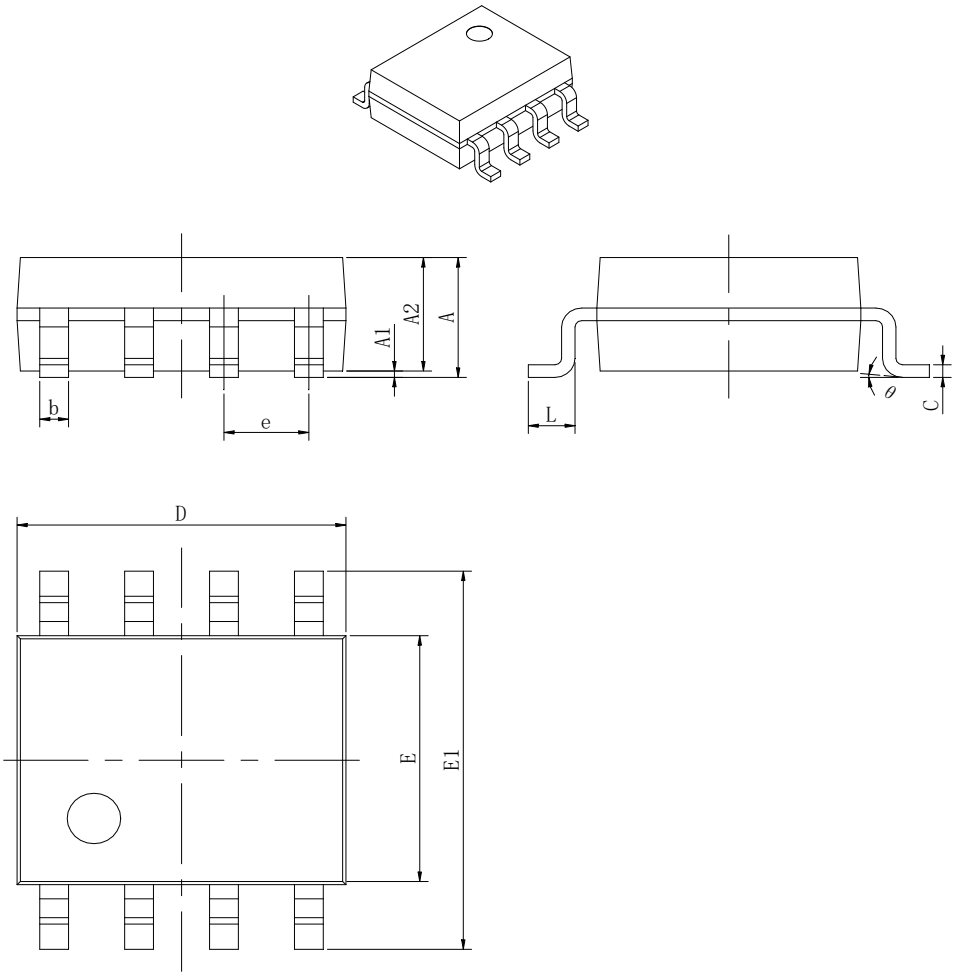
Constant current voltage: 2V

Resistance: R

R= (DC-2V-Vled×n) ÷ Iout

For example, system power supply: DC24V, single LEDbreakover voltage drop: 2V, number of series LED: 6, constant current value: 14mA, calculated according to the above formula: R= (24V-2V-6V×2)÷17 mA≈750Ω. Only need to connect in series about 750Ω resistance at OUT port.

Packaging diagram (SOP 8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

(All specs and applications shown above are subject to change without prior notice.)