WS2805

Single-wire 256-level grayscale five-channel constant current LED driver IC

Main features • The OUTR, G, B, W1, and W2 ports have a voltage resistance of 20V, and the DIN and DOUT ports have a voltage resistance of 24V. • The chip has a built-in voltage regulator tube. The power supply terminal below 24V only needs to connect a resistor to the VDD pin, without the need for an external voltage regulator tube. • The chip has built-in resistors, and the DIN and DOUT ports have overvoltage protection. Short-circuiting to 24V will not cause burnout. • Built-in signal shaping circuit, any IC receives the signal and then outputs it after waveform shaping, ensuring that line waveform distortion will not accumulate. • Built-in power-on reset and power-off reset circuit. • The PWM control terminal can achieve 256 levels of adjustable grayscale and a scanning frequency of 4KHz. • Serial interface cascade interface can receive and decode data through one signal line. • Resume downloading at breakpoints. Even if a single chip is damaged, the overall display effect will not be affected. • The transmission distance between any two points does not exceed 5 meters without adding any circuits. • When the refresh rate is 30 frames/second, the number of cascades is not less than 1024 points. • Data transmission speed can reach 800Kbps.

Main application areas • LED point light sources, LED light strings, and LED modules. • LED soft light strips, hard light strips, LED guardrail tubes. • Various electronic products and electrical equipment marquees. • Various other LED lighting products.

product description

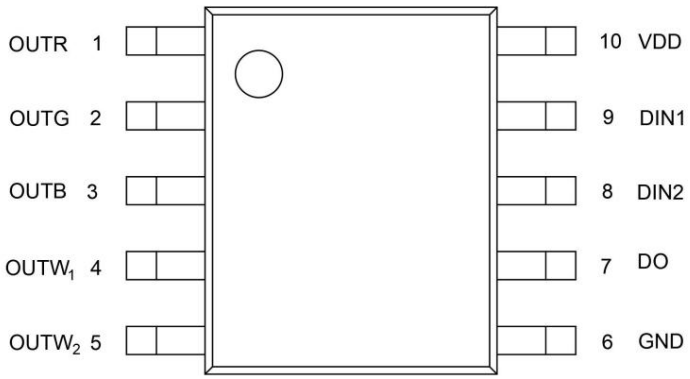
WS2805 is a five-channel LED drive control dedicated circuit. The chip contains an intelligent digital interface data latch signal shaping amplification drive circuit, a high-precision internal oscillator and a 20V high-voltage programmable constant current output driver. At the same time, in order to reduce the power ripple, OUTR, G, B, The W1 and W2 channels have a delayed turn-on function, which can reduce circuit ripple during frame refresh.

The chip uses a single-wire return-to-zero code communication method. After the chip is powered on and reset, the DIN1 terminal accepts the data transmitted from the controller and first sends it After the incoming 40-bit data is extracted by the first chip, it is sent to the data latch inside the chip. The remaining data is reshaped and amplified by the internal shaping processing circuit and then forwarded and output to the next cascaded chip through the DO port. Each time it passes through For chip transmission, the signal is reduced by 40 bits. The chip uses automatic shaping and forwarding technology, so that the number of cascades of the chip is not limited by signal transmission, only the signal transmission speed requirements.

The data latch inside the chip generates different duty cycle control signals at the OUTR, G, B, W1, and W2 control terminals based on the received 40-bit data. number, when waiting for the DIN terminal to input the RESET signal, all chips will send the received data to each segment synchronously. The chip will re-receive the data after the signal ends. After receiving the first 40 bit data, it will forward the data port through the DO port. , before the chip receives the RESET code, OUTR, G, B, The original output of the W1 and W2 pins remains unchanged. After receiving the low-level RESET code of more than 280ÿs, the chip will output the 40bit PWM data pulse width just received to the OUTR, G, B, W1, and W2 pins.

Available in SOP-10 package.

Pinout arrangement



Pinout function

serial number	symbol	Pin name	Function description
1	OUTR	LED driver output	RED (red) PWM control output
2	OUTG	LED driver output	GREEN (green) PWM control output
3	OUTB	LED driver output	BLUE (blue) PWM control output
4	OUTW1	LED driver output	WHITE1 (white) PWM control output
5	OUTW2	LED driver output	WHITE2 (white) PWM control output
6	GND	land	Signal ground and power ground
7	DO	data output	Show data cascade output
8	DIN2	Data 2 input	Display data 2 input
9	DIN1	Data 1 input	Display data 1 input
10	VDD	Logic power	IC power supply

Maximum rating (TA=25ÿ, VSS=0V)

parameter	symbol	scope	unit
Logic supply voltage	VDD	+3.5~+5.7	V
R, G, B, W1, W2 output port voltage resistance	VOUT	20	V
Logic input voltage	VI	VDD-0.7ÿVDD+0.7V	V
Operating temperature	Topt	-40ÿ+85	ÿ
Storage temperature	Txt	-40~+105	ÿ

Electrical parameters (TA=25ÿ, VDD=4.5ÿ5.5V, VSS=0V)

parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Quiescent Current	Io	——	0.6		——mA	DC=5V
R, G, B, W1, W2 Low level output current	IOL	10	12	14	mA	DC=5V, DINÿFFHÿ
Low level output current	Idout	10	————mA			Vo=0.4V, DOUT
Signal input current	II	———		±1	μA	VI=VDD/VSS
High level input	VIH	0.7VDD ————			V	DIN
low level input	VIL ——	0.3 VDD			V	DIN
hysteresis voltage	VH	——	0.35 ——		V	DIN

Switching characteristics (TA=25ÿ, VDD=4.5ÿ5.5V, VSS=0V)

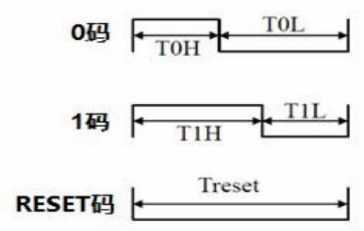
parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Oscillation frequency	*Fosc* ——800			——KHz		——
Transmission delay time	tPLZ ——	——	300		ns	CL=15pF, DINÿDOUT, RL=10Kÿ
Fall time	tTHZ ————		120		μs	CL=300pF, OUTR/OUTG/OUTB
Data transfer *rateFMAX*		600 ——	——	Kbps duty cycle 50%		
Input capacitance	CI ————		15		pF	——

Data transfer time

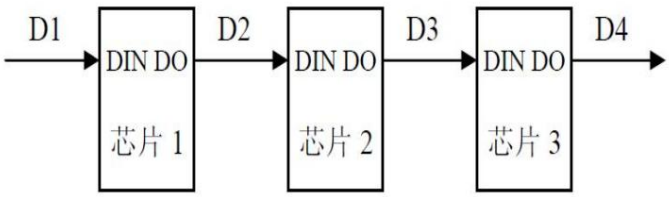
T0H	0 code, high level time	220ns~380ns
T1H	1 code, high level time	580ns~1us
T0L	0 code, low level time	580ns~1us
T1L	1 code, low level time	580ns~1us
RES	Frame unit, low level time	280μs or more
TDATA	Data cycle (TH+TL)	ÿ1.25us

Timing waveform diagram

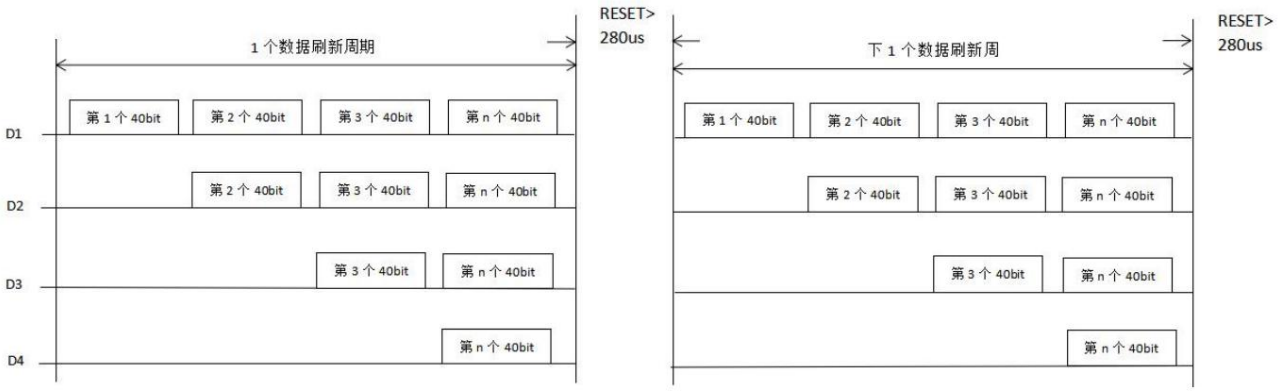
Input pattern:



connection method:



Data transfer method



Note: D1 is the data sent by the MCU, and D2, D3, and D4 are the data automatically shaped and forwarded by the cascade circuit.

40bit data structure

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	…continue…

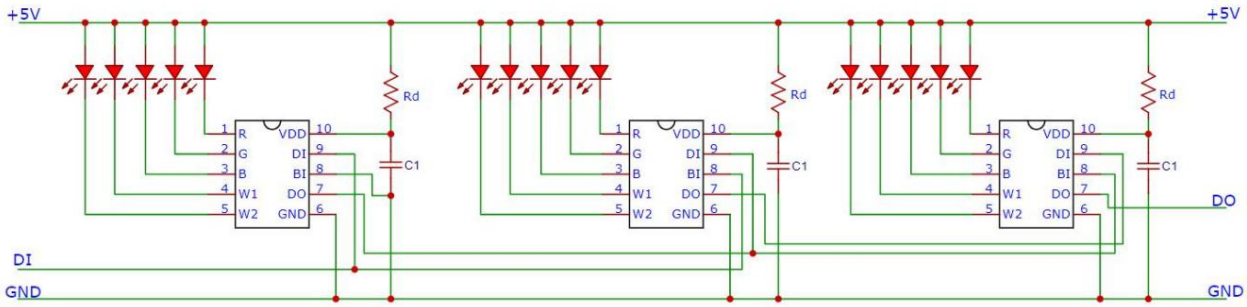
…continued from…	B7	B6	B5	B4	B3	B2	B1	B0	W17	W16	W15	W14	W13	W12	W11	W10					…continue…

…continued from…	W27	W26	W25	W24	W23	W22	W21	W20

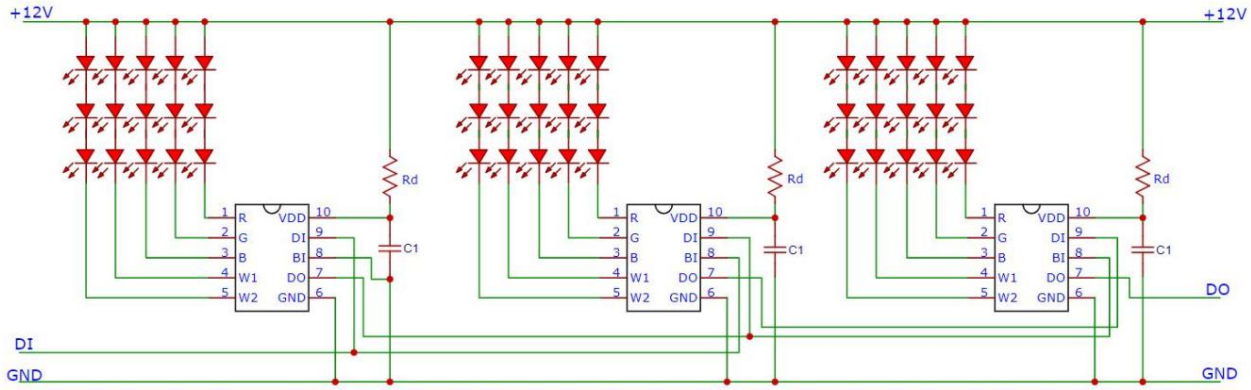
Note: The high bit is sent first, and data is sent in the order of RGBW1W2.

Typical application circuit

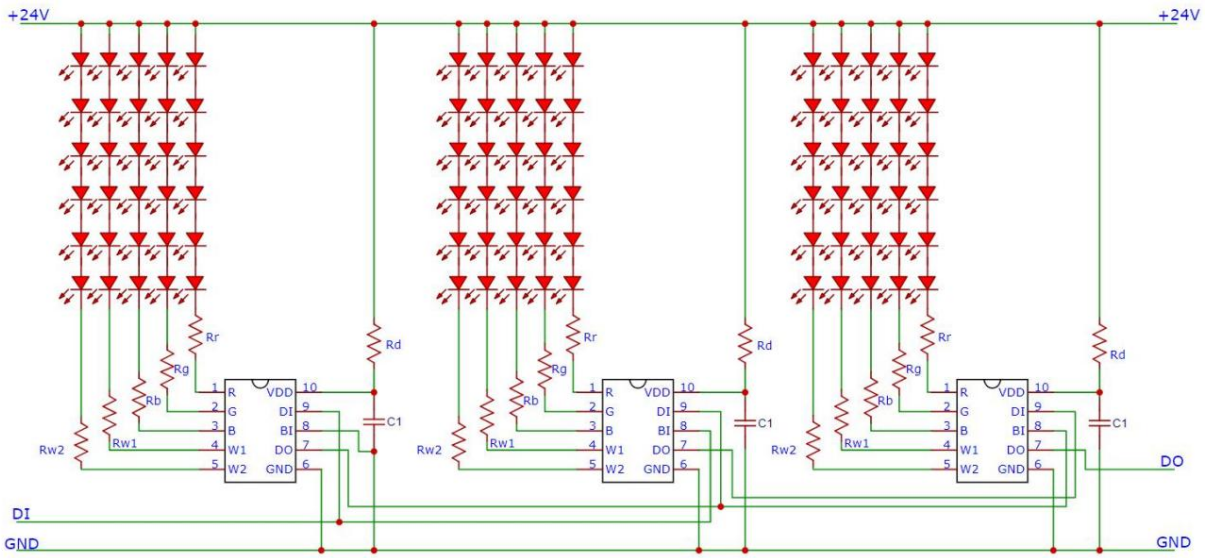
1. 5V power supply application reference circuit (with **1** LED per channel): The recommended value for **Rd** is 150R, and the recommended value for **C1 is 1uf.**



2. Reference circuit for 12V power supply application (with **3** LEDs per channel): The recommended value for **Rd** is 4.7k, and the recommended value for **C1 is 1uf.**

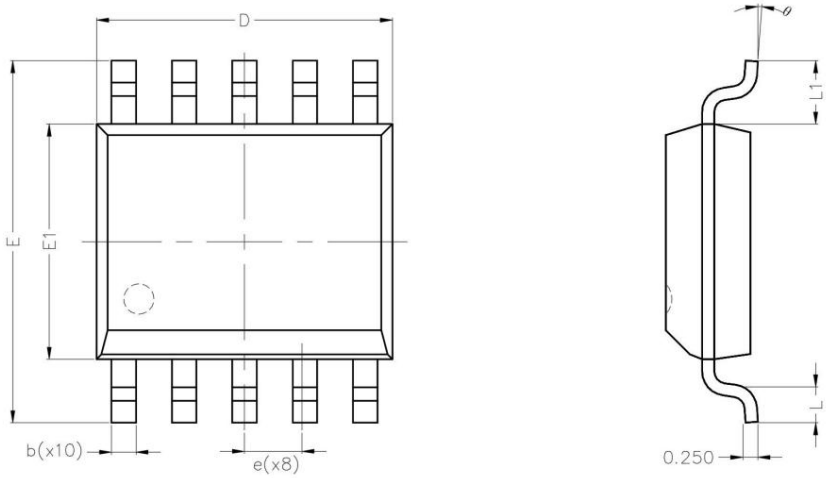


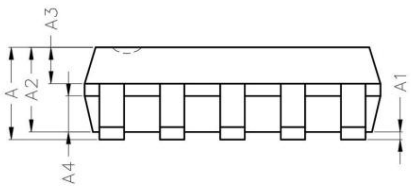
3. 24V power supply application reference circuit (each channel has **6** LEDs): The recommended value for **Rd** is 10k, and the recommended value for C1 **is 1uf.**



Package diagram and parameters

ÿ **SOP-10** package





	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	–	–	1.75
STAND OFF	A1	0.05	0.125	0.20
MOLD TOTAL THICKNESS	A2	1.30	1.40	1.60
TOP MOLD THICKNESS	A3	0.55	0.60	0.65
BOTTOM MOLD THICKNESS	A4	0.547	0.597	0.647
LEAD WIDTH	b	0.31	–	0.53
MOLD LENGTH	D	4.80	4.90	5.00
MOLD WIDTH	E1	3.80	3.90	4.00
LEAD SPAN	E	5.80	6.00	6.20
LEAD PITCH	e	1.00 BSC		
LEAD LENGTH	L1	0.95	1.05	1.15
LEAD SOLE LENGTH	L	0.40	0.60	0.80
LEAD FORM ANGLE	θ	0°	–	8°

File change history

Version number	status	Edit summary	Revision Date	Revisor	Approver
V0.1	N	New (first version of development)	20230210	Yu Xinghui	Yin Huaping
V0.2	M	Parameters updated, renamed WS2805	20230322	Yu Xinghui	Yin Huaping
V0.3	M	Pin definition adjustment, package size adjustment	20230324	Yu Xinghui	Yin Huaping

Note: The development version is engineering batch test data and is an informal mass production version. Various parameters may be optimized and are for reference only.

The official mass production first version is V1.0.